University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #2 – Solution
August 8, 2007

Name _____

Perm # _____

Lab Section _____

Problem #1 (25 points) _____

Problem #2 (25 points) _____

Problem #3 (25 points) _____

Problem #4 (25 points) _____

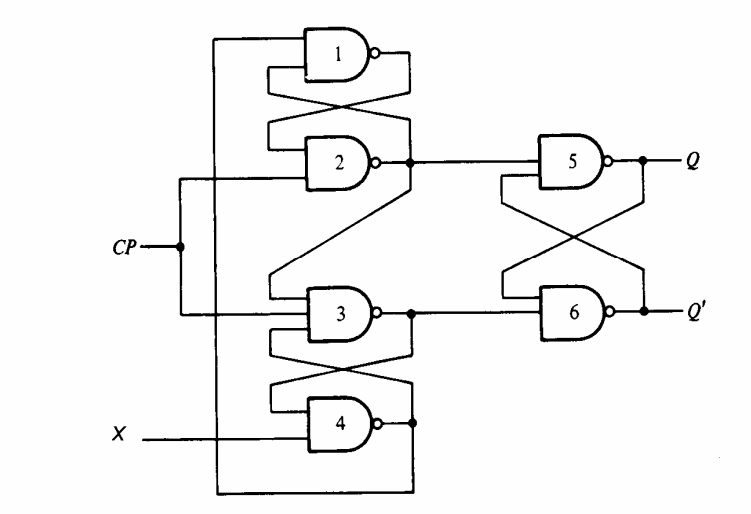
Total (100 points) _____

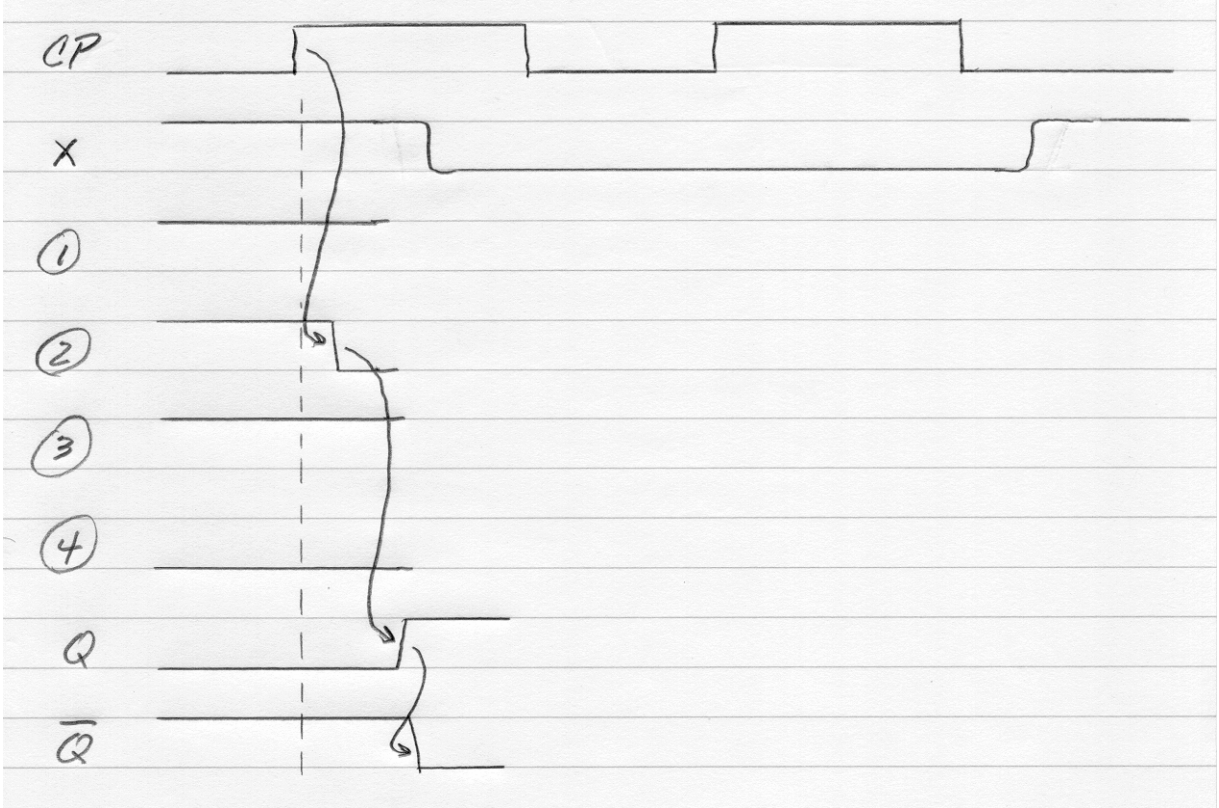
- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions on the exam.

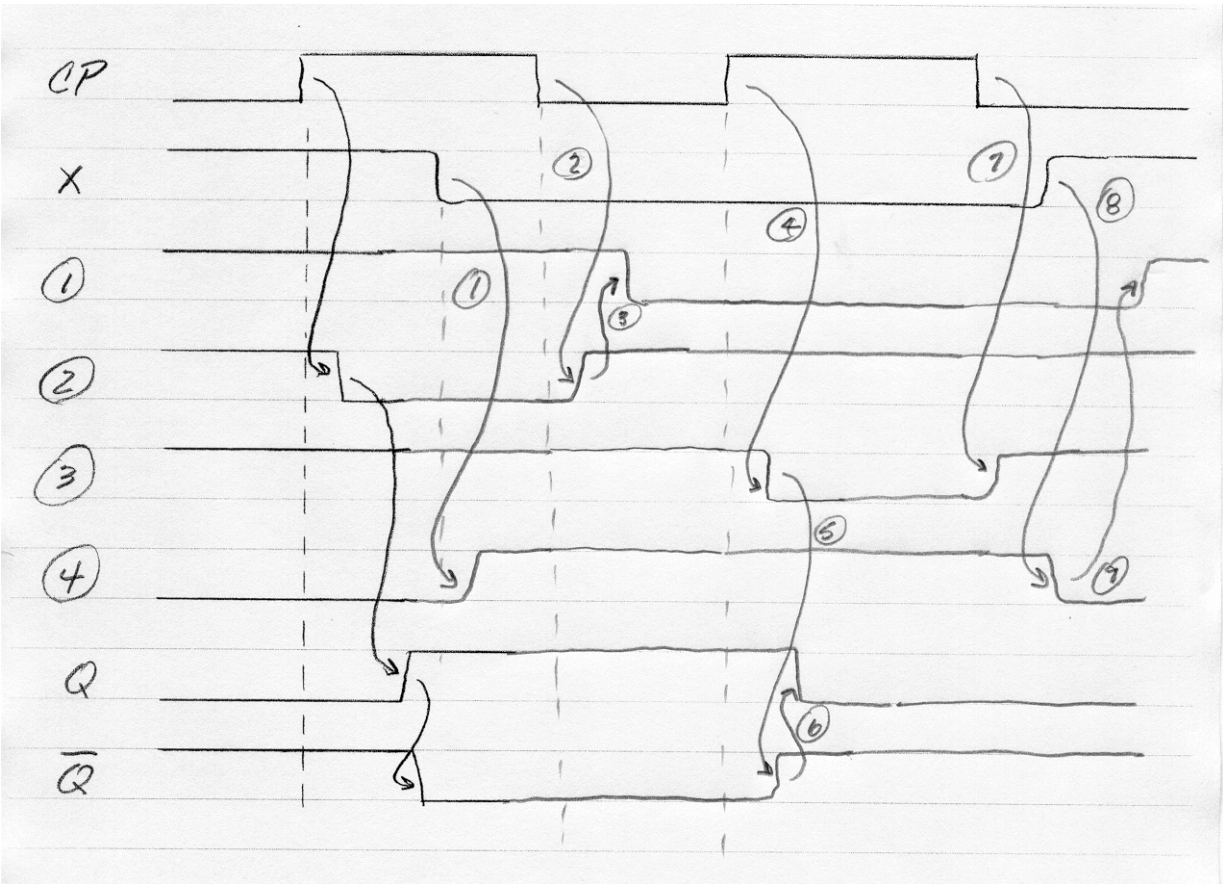
Problem #1.

Complete the timing diagram (on the following page) for the circuit shown below. Assume all gate delays are equal and all are much shorter than the clock period. You can also assume that both setup and hold times are satisfied.

I'm more interested in the order of transitions (indicated by arrows, as shown on the timing diagram), than the detailed timing numbers.



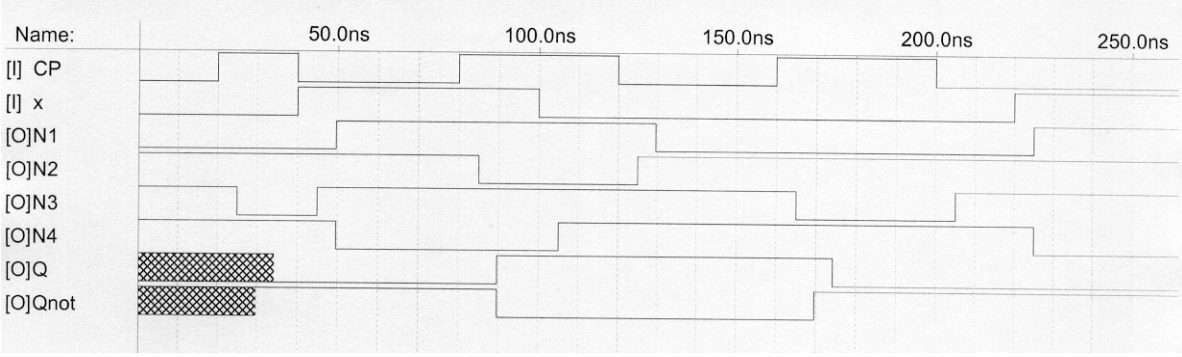

CP
X
1
2
3
4
Q
$\overline{Q}$

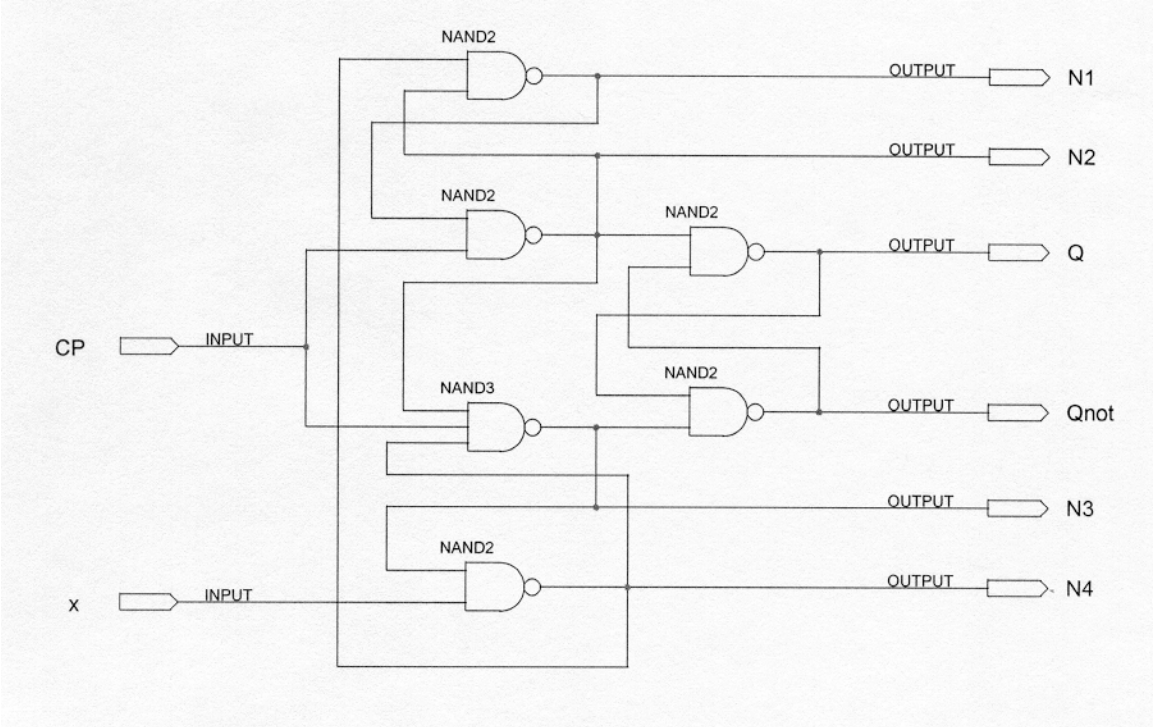


2 points:	transition 1
4 points total:	transitions 2 and 3
13 points total:	transitions 4, 5 and 6… this is the most important part, resetting the flip flop to 0 on the positive edge of the clock
2 points:	transition 7
4 points total:	transitions 8 and 9

25 points total

Simulation results:





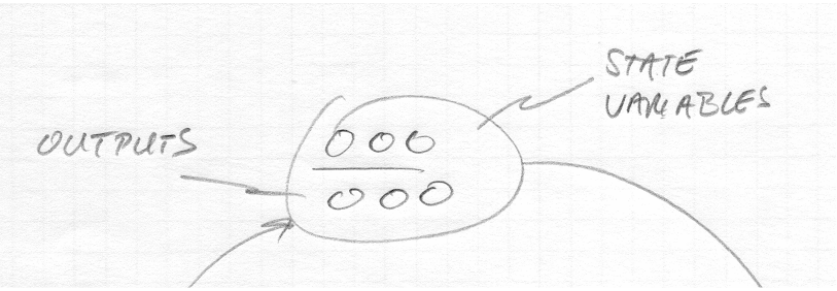
Problem #2.

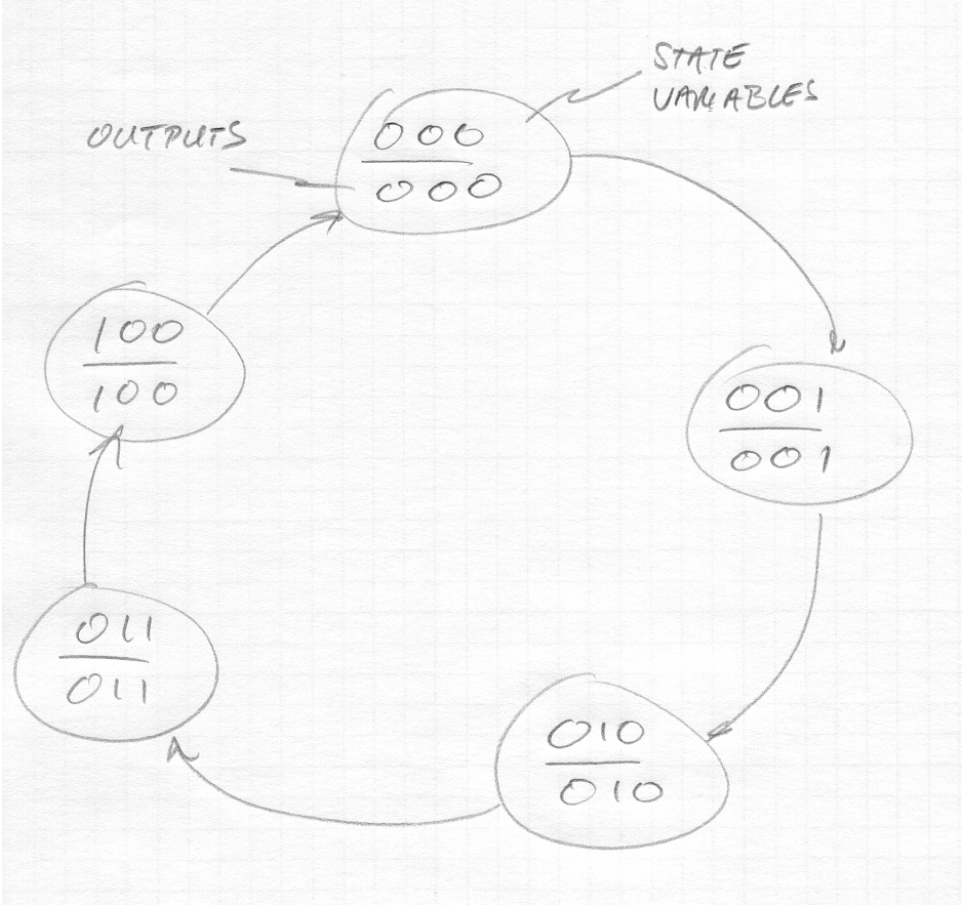
In this problem, you are to design a 3-bit counter which can function as either a modulo 5 counter (0,1,2,3,4,0…) or a Fibonacci Sequence counter (0,1,1,2,3,5,0...), based on a single input B. When B is high the counter counts in binary (mod 5); when B is low the counter sequences through the first 6 Fibonacci numbers.

If the B input changes, the next value of the counter should be next greater number for the new sequence. For instance, if the counter is at binary 3 and B goes low, the next output should be 5 (Fibonacci count). Similarly, if the counter is at Fibonacci 3 and B goes high, the next output should be 4 (binary count).

1. (3 points) Construct the state diagram for the binary (mod 5) portion of the counter. Assume for this part that the input B is always high; we'll add the Fibonacci capability later.

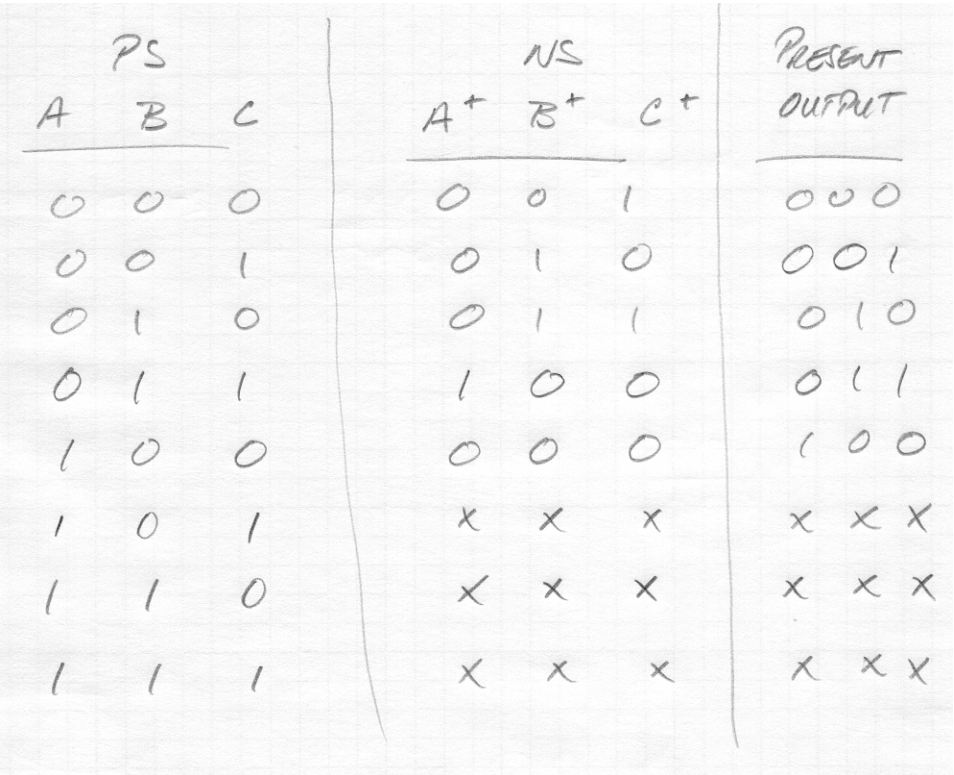
   For each state, include the binary encoding of the state is (the values of state variables A, B and C) and the three bit numerical output (they can be the same) on the state diagram as shown below for state 0 0 0 and output = 0 0 0.




STATE VARIABLES
OUTPUTS
000
000
001
001
010
010
011
011
100
100

2. (4 points) Construct the state table for the design specified in part 1 above. The table should be in the form:

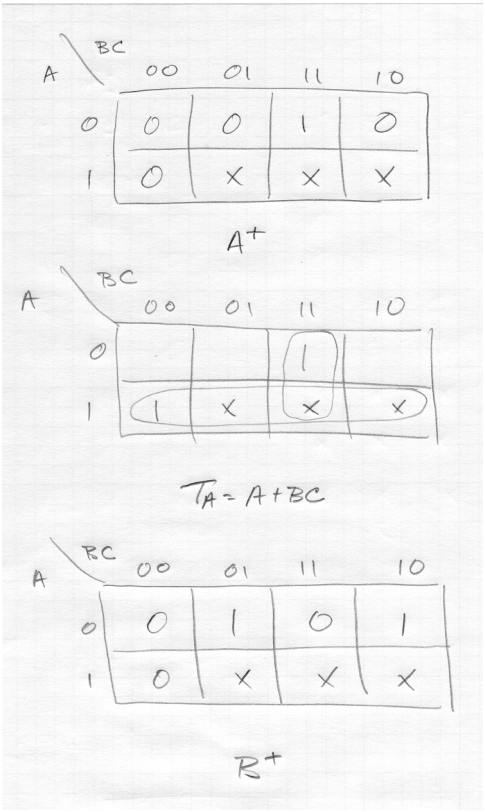
PS			NS			Present
A	B	C	A	B	C	Output
0	0	0	0	0	1	0 0 0

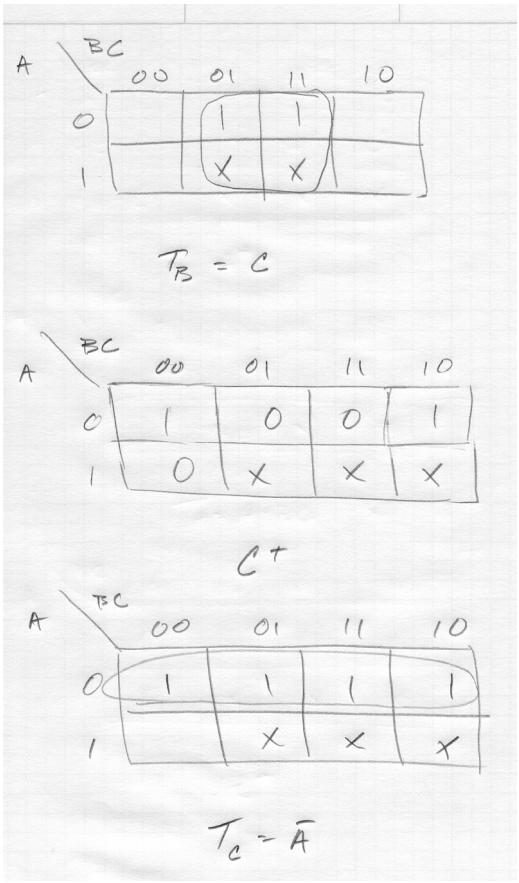


PS			NS			PRESENT
A	B	C	A^+	B^+	C^+	OUTPUT
0	0	0	0	0	1	0 0 0
0	0	1	0	1	0	0 0 1
0	1	0	0	1	1	0 1 0
0	1	1	1	0	0	0 1 1
1	0	0	0	0	0	1 0 0
1	0	1	x	x	x	x x x
1	1	0	x	x	x	x x x
1	1	1	x	x	x	x x x

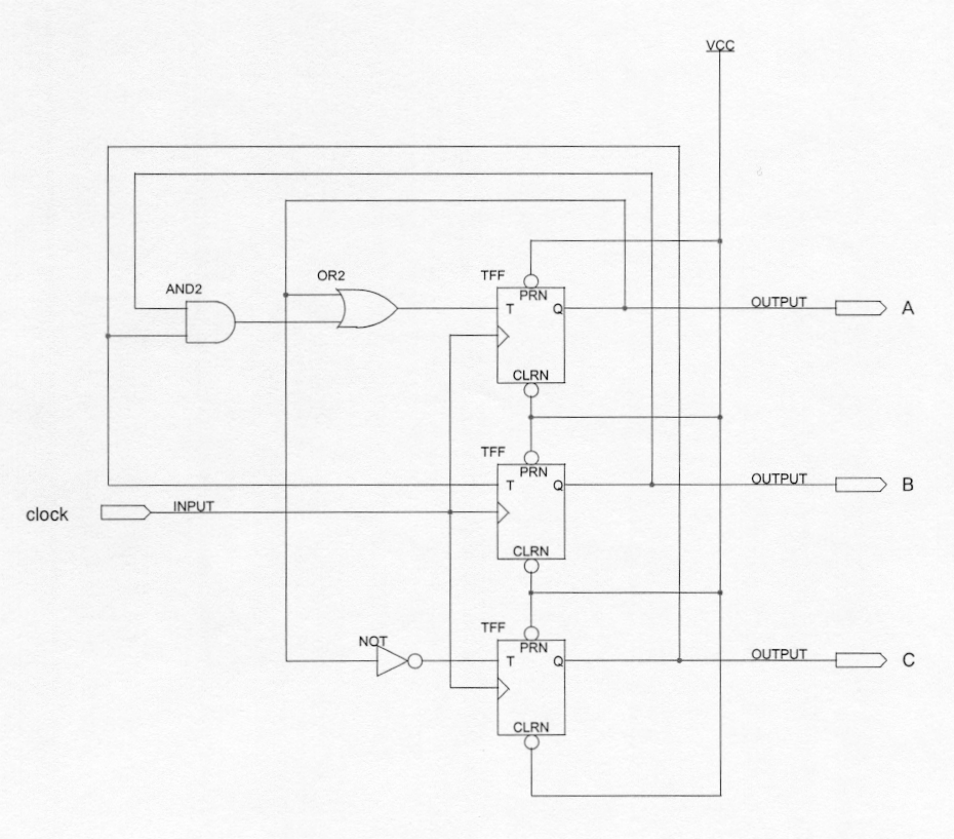
4 points; note next state, don't cares and correct present output.

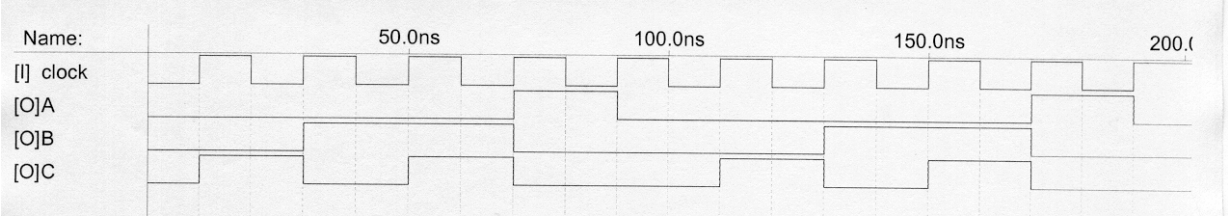
3. (5 points) If we were to implement this design with edge triggered T flip flops, what would the T inputs to the three flip flops be (T_A, T_B, T_C)? Include both next State Maps and T Flip Flop input (excitation) maps in your answer.





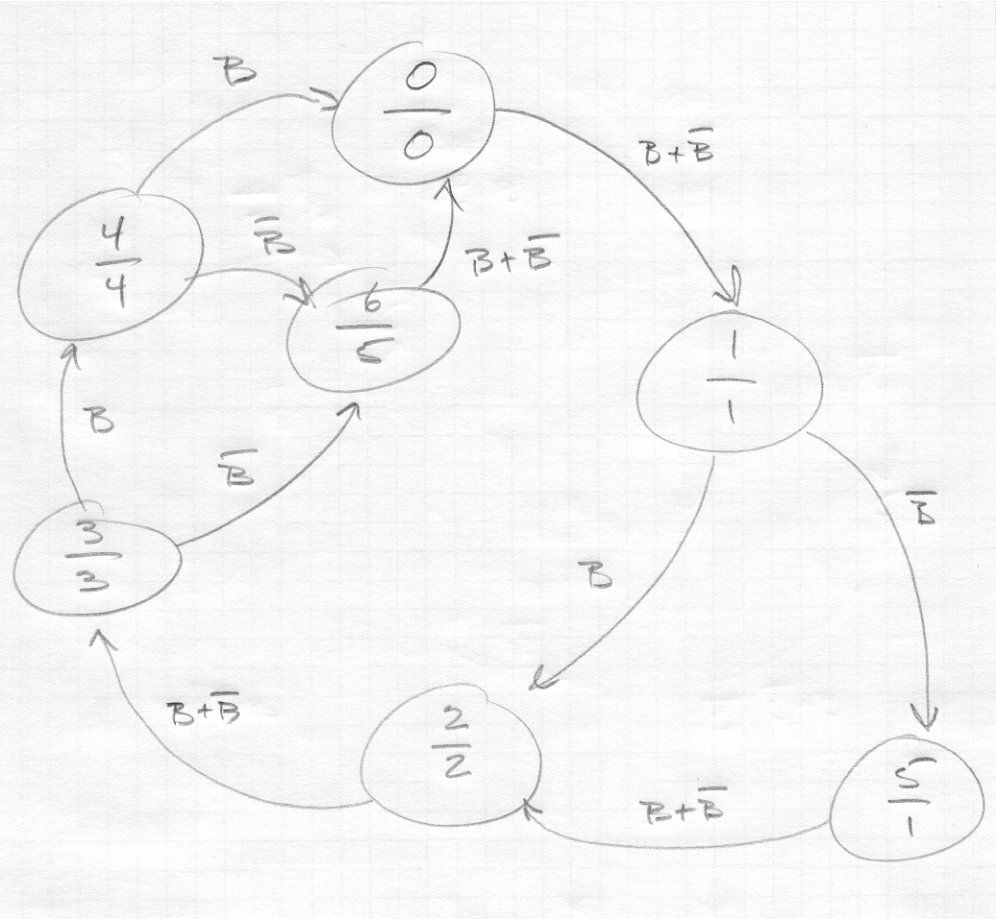
Simulation results:





4. (10 points) Now complete the design by adding the capability to count the first 6 Fibonacci numbers. Construct a state diagram and indicate the decimal (or binary) value of the state variables, A, B and C and the decimal (or binary) value of the output number associated with that state.

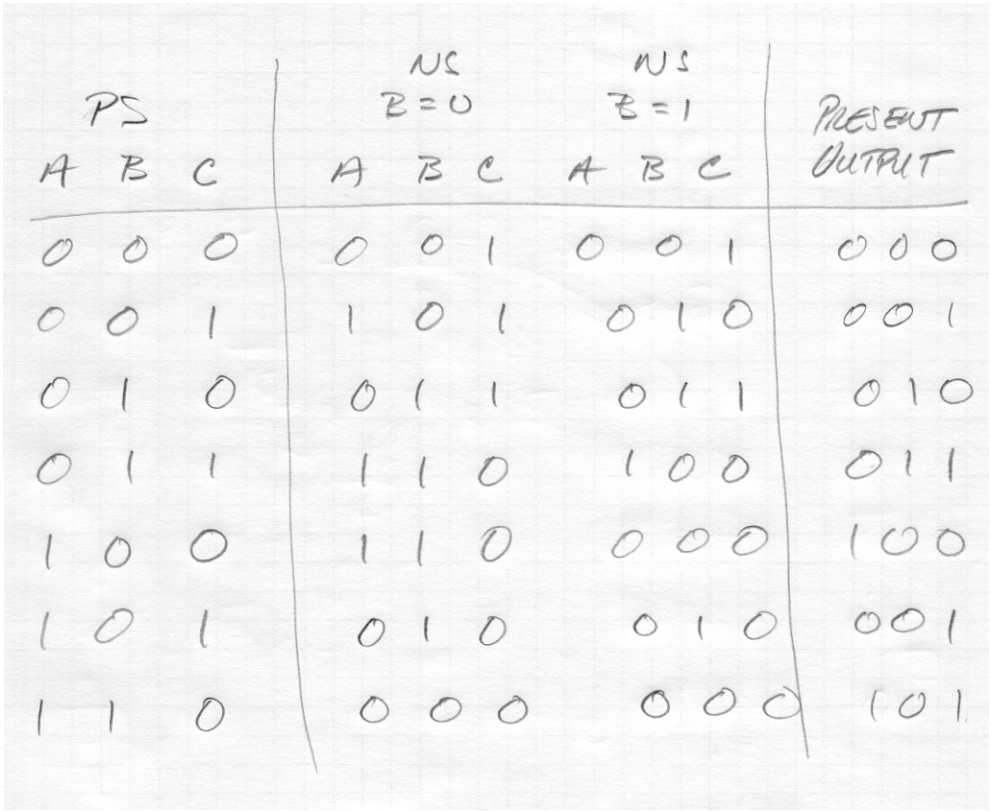
   (Hint: Note that the Fibonacci sequence repeats the number 1. For this problem, assume that a 3 input, 3 output combinational circuit is available to translate the values of the current state variables to a numerical output; i.e., this is a Moore machine).



There are 10 correct transitions in the state diagram; 1 point per correct transition.

5. (3 points) Construct the state table for the state diagram with the derived in part 4 above. It should be in the form:

PS			NS, B=0			NS, B=1			Present
A	B	C	A	B	C	A	B	C	Output
0	0	0	0	0	1	0	0	1	0 0 0



PS			NS B=0			NS B=1			PRESENT OUTPUT
A	B	C	A	B	C	A	B	C	
0	0	0	0	0	1	0	0	1	0 0 0
0	0	1	1	0	1	0	1	0	0 0 1
0	1	0	0	1	1	0	1	1	0 1 0
0	1	1	1	1	0	1	0	0	0 1 1
1	0	0	1	1	0	0	0	0	1 0 0
1	0	1	0	1	0	0	1	0	0 0 1
1	1	0	0	0	0	0	0	0	1 0 1

state table should also have:

1	1	1	|	x	x	x		x	x	x	|	x	x x

3 points, mostly the output = 1 for two different states

Problem #3.

In this problem you are asked to design a synchronous 4-bit, up / down counter with parallel load capability (load all four bits synchronously) and an asynchronous reset (all bits asynchronously set to 0) using Verilog.

The register can perform the following synchronous functions, based on a 2 bit input (F1, F0).

00	Hold (register contents remain unchanged)
01	Increment
10	Decrement
11	Load from external inputs (inputs are labeled D3 : D0)

The contents of the register are labeled Q3 : Q0 and the low true, asynchronous reset signal is labeled Rn.

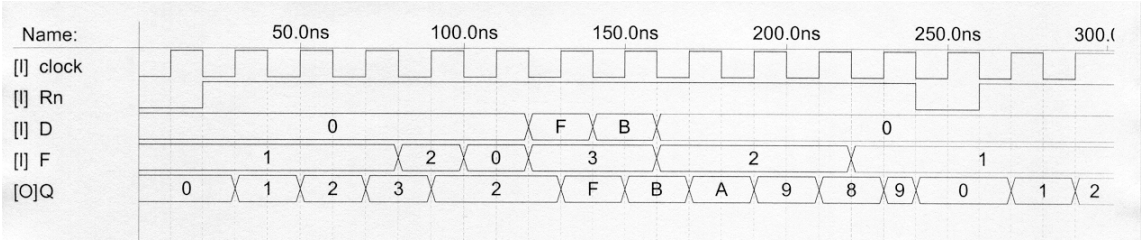
Your solution doesn't have to be precisely, syntactically correct, but all the elements should be present. Your design should be simple, straightforward and easily understood by an experienced Verilog designer.

```
module mid2register (clock,Rn,D,F,Q);

input clock,Rn;
input [3:0]D;
input [1:0]F;
output [3:0]Q;
reg [3:0]Q;

always @ (negedge Rn or posedge clock)
   begin

        if (!Rn)
                        Q <= 0;

        else
                case(F)

                        1 : Q <= Q + 1;
                        2 : Q <= Q - 1;
                        3 : Q <= D;

                        default :  Q <= Q;

                endcase

   end
endmodule
```

5 points for module declaration
5 points for vector, input and output declarations
5 points for always declaration (both signals on edge)
5 points for correct implementation of reset (asynchronous and priority)
5 points for case statement

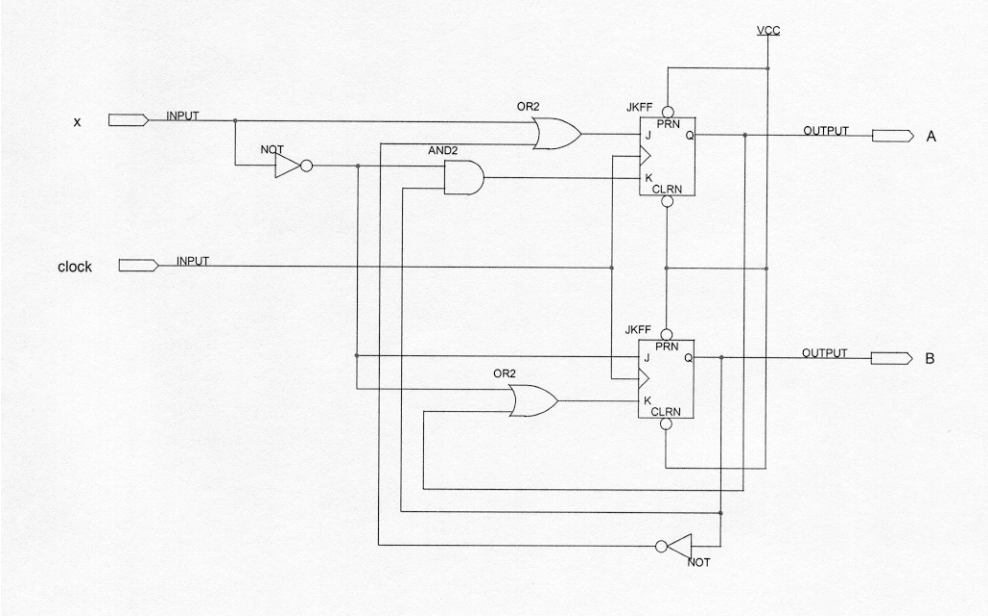
In all cases, simplicity is the key; the more convoluted, the fewer points.

Simulation results:



Problem #4.

A finite state machine is constructed using positive edge triggered, JK flip flops as shown in the schematic below:



1. (2 points) What are the J and K inputs to the A and B flip flops: J_A, K_A, J_B, K_B, (if you get this wrong, the rest of your answer will be wrong).

$J_A = X + B'$

$K_A = X'B$

$J_B = X'$

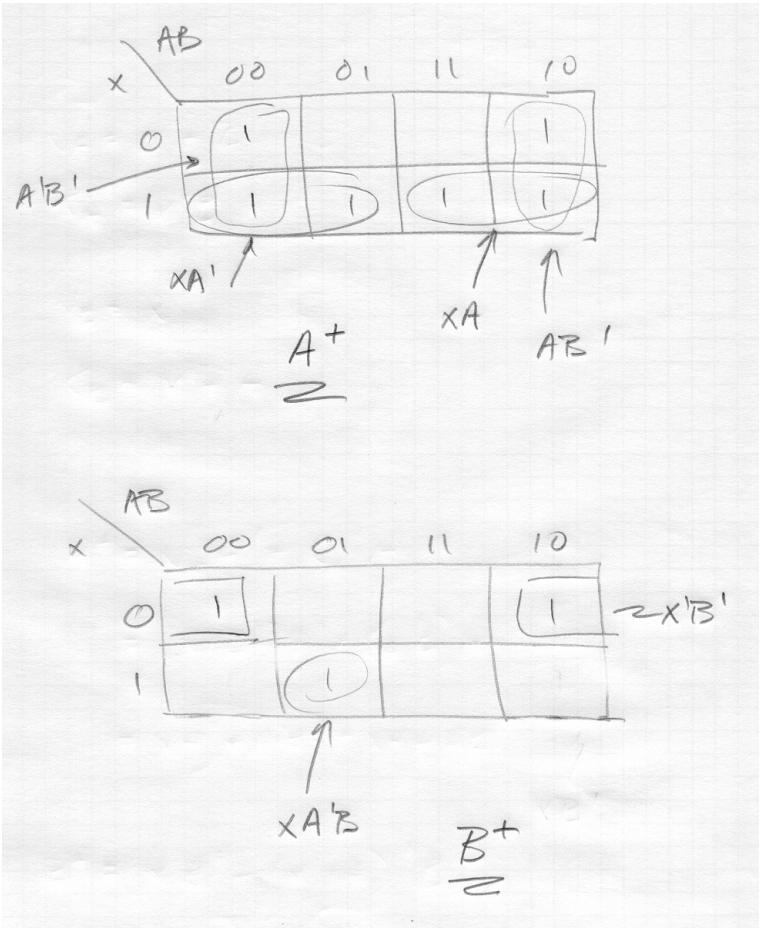
$K_B = X' + A$

2. (12 points) Derive next state equations for the flip flops (recall the characteristic equation for a JK flip flop is Q+ = JQ' + K'Q).

$$A^+ = J_A A' + K_A' A$$
$$= (x + B')A' + (x'B)'A$$
$$= xA' + A'B' + xA + AB'$$

$$B^+ = x'B' + (x' + A)'B$$
$$= x'B' + xA'B$$

3. (5 points) Map the next state equations onto K maps.



4. (3 points) Construct a state table for the machine.

A	B	x=0 A+	x=0 B+	x=1 A+	x=1 B+
0	0	1	1	1	0
0	1	0	0	1	1
1	1	0	0	1	0
1	0	1	1	1	0

5. (3 points) Construct a state diagram for the machine.